

Abstract

A large part of today's multi-core chips is interconnect. Increasing communication complexity has made new strategies for interconnects essential such as Network on Chip. Power dissipation in interconnects has become a substantial part of the total power dissipation. Hence, techniques to reduce interconnect power have become a necessity. In this thesis, we present a design methodology that gives values of bus width for interconnect links, frequency of operation for routers, in Network on Chip scenario that satisfy required throughput and dissipate minimal switching power. We develop closed form analytical expressions for the power dissipation, with bus width and frequency as variables and then use Lagrange multiplier method to arrive at the optimal values.

To validate our methodology, we implement the router design in 90 nm technology and measure power for various bus widths and frequency combinations. We find that the experimental results are in good agreement with the predicted theoretical results.

Further, we present the scenario of an Application Specific System on Chip (ASSoC), where the throughput requirements are different on different links. We show that our analytical model holds in this case also. Then, we present modified version of the solution considered for Chip Multi Processor (CMP) case that can solve the ASSoC scenario also.